ELLIOTT 900

Volume 1: FUNCTIONAL SPECIFICATION

Part 2: THE BASIC 900 COMPUTER UNIT

Section 7: 900 STANDARD PERIPHERAL INTERFACE.

Contents

END-OF-TEXT FIGURES

Chapter 1: INTRODUCTION

1.1 General

A standard interface is set of pre-defined signal lines. This concept facilitates the design of units that have to operate together. The 900 computer has a standard peripheral interface across which the central processor communicates with its peripheral.

Any peripheral device designed to match the 900 Standard Peripheral Interface may be connected direct; peripherals with a 4100 interface or with an NPL interface may be connected via the appropriate 900 Interface Matching Unit. The peripheral interface signal lines operate one peripheral, where more than one peripheral is required a Multiplexer Unit (see Section 1.3.1) is connected between the peripheral interface and the peripherals, this increases the power of the signal lines and provides sockets for up to eight peripherals.

The 900 Standard Peripheral Interface has 63 signal lines used as follows:-

DATA OUT, 18 lines, used to transfer complete 18 bit words from the computer to the peripheral.

DATA IN, 18 signal lines, used to transfer complete 18 bit words from the peripheral to the computer.

Address, 11 signal lines, these carry the less significant binary digits of the address part of the input or output instruction. They select a peripheral and detail the operations to be performed.

Select, 2 signal lines, these specify, input or output transfer and are set by the central processor as specified by bit 13 of the instruction address (see also paragraph 3.4.2).

INTERRUPT, 3 signal lines, used by the peripheral to interrupt the computer on a priority system.

REPLY used by the peripheral to indicate when the data lines have been served.

BLOCK TRANSFER and LAST WORD, signals from the computer associated with input/output transfers.

Miscellaneous, four signal lines and four unused spare lines.

The 900 teleprinter paper tape reader and paper tape punch are connected to an interface which is basically the same as the peripheral interface but has only eight input, eight output and four address signal lines.

Chapter 2: TRANSFERS

2.1 Two types of transfer are provided for:

(1) Single word, one 18-bit word is transferred by a single instruction (Function 15, address range 0 to 6159) to or from the accumulator register.

(2) Block transfer, a series of 18-bit words is transferred by a single instruction (Function 14, address range 2048 to 6143) to or from a series of consecutive store locations. The first store location used and the number of words to be transferred are programmed into the A and Q registers respectively prior to the block transfer instruction. The contents of Q are integers within the range 0 to 4096.

NOTE: If the Q register is loaded by means of a Ø instruction which immediately precedes the 14 instruction, then no interrupt can occur between these two instructions. This is of value if interrupt routines are in use which fail to preserve the least significant bit of Q.

Chapter 3: INTERFACE SIGNAL LINES

3.1 General.

All interface lines carry binary signals, the states of these are described as 1 or 0 if the line carries a digit of a binary number and as true or false if the signal has a logical function.

3.2 DATA IN lines.

There are eighteen DATA IN lines. These carry complete 18 bit words transferred from the peripheral to the accumulator by input instructions. The peripheral must place data on the DATA IN lines only when ADDRESS, in conjunction with INPUT SELECT or BLOCK TRANSFER, indicate that it is addressed by the current instruction. The DATA IN lines will be zero when the peripheral is not selected by the ADDRESS lines, also they will be zero when the peripheral sets REPLY true when INPUT SELECT is false (i. e. for an output function).

3.3 DATA OUT lines

There are eighteen DATA OUT lines, these carry complete 18 bit words transferred from the accumulator to the peripheral by output instructions. They are significant only while OUTPUT SELECT is true. Their significance at all other times is undefined.

3.4 ADDRESS lines

3.4.1 There are eleven address lines, these carry bits 1 to 11 of the address part of the instruction and are used to select the peripheral device and to detail the operation to be performed.

The address lines are significant only while OUTPUT SELECT, INPUT SELECT or BLOCK TRANSFER is true. Their significance at all other times is undefined.

3.4.2 The central processor determines from the instruction function bits 17-14 and address bit 13 whether it is:

(1) an input or output instruction, or

(2) a single or block transfer, and

(3) from address bit 12 whether it is a peripheral or paper tape instruction.

Using this information the central processor sets true the relevant interface signals.

3.5 INPUT SELECT

This signal is set true by the central processor when an input transfer instruction is performed. The peripheral selected by the instruction address bits 1-11 places a word on the DATA IN lines when this line is set true. Having done this the peripheral sets true the REPLY line to the central processor.

INPUT SELECT is set false by the central processor when it has received REPLY true and has read the DATA IN lines. It remains false at all other times.

3.6 OUTPUT SELECT

This signal is set true by the central processor when an output transfer instruction is performed. The peripheral selected by the instruction address bits 1-11 will read the word on the DATA OUT lines and then set true the REPLY line to the central processor.

OUTPUT SELECT is set false by the central processor when it receives REPLY true. It remains false at all other times.

3.7 REPLY

This signal to the central processor is set true by the peripheral when:-

(1) for an input transfer, the peripheral has placed a word on the DATA IN lines. The central processor will not read the DATA IN lines until REPLY is set true.

(2) for an output transfer, the peripheral has read the word on the DATA OUT lines.

In both cases the central processor will stop, with the relevant SELECT signal true, until the peripheral sets REPLY true.

REPLY is set false by the peripheral as soon as possible after the SELECT signal becomes false and remains so at all other times.

The peripheral can only set REPLY true if the ADDRESS lines indicate that it is the particular device addressed by the current instruction.

3.8 BLOCK TRANSFER

This signal is set true by the central processor to indicate the commencement of a block transfer operation. It is set true before the relevant SELECT signal is set true for the first transfer. It remains true until the end of a block transfer i. e. until after SELECT has become false after the LAST WORD transfer.

3.9 LAST WORD

This signal is set true by the central processor when the last word of a block transfer is being transferred. It is true for the duration of the relevant SELECT signal for this transfer, and false while SELECT is true for all other transfers in the block transfer.

Its significance when SELECT is false and for a single transfer is undefined.

3.10 INTERRUPTS

There are three INTERRUPT lines from the peripheral to the central processor; they are INTERRUPT1, INTERRUPT2 and INTERRUPT3. One (or more) is made true when the peripheral requires the central processor to enter the program at that level (1, 2 or 3 respectively), the higher priority program being entered if more than one level of INTERRUPT is given. The relevant INTERRUPT line must be held true for at least 15μs and should be made false before the termination of the entered program, if it is not made false the program will be re-entered.

3.11 RESET

This line from the central processor carries the logical signal RESET which becomes true for at least 100 ms when the central processor is switched on, or when the control panel RESET button is operated, and typically 20 ms if the central processor switches itself off due to some fault condition. It will be made false as soon as the central processor starts obeying.

This signal may be used to reset the peripheral device to its initial state.

3.12 POWER ON

This line is energised when power is applied to the central processor logical circuitry and de-energised when power is removed.

3.13 Spare lines

There are four spare lines.

Chapter 4: EQUIPMENT DESIGN: TIMING REQUIREMENTS

These timing requirements do not refer to any particular 900 series computer or peripheral: they are limiting design requirements which all 900 series peripherals and computers must meet. In the case of synchronously operated devices, which will fail if a response is not received within a limited time, the performance of the particular computer concerned must also be considered, as a minimum data transfer rate is not specified or implied.

Equipment should be designed to meet these requirements and to work satisfactorily with other equipments designed to meet these requirements.

4.1 Single word input (see Figure 1)

(1) Computer

The ADDRESS signals must be in the correct state at least 200 ns before INPUT SELECT is set true and must remain correct until 200 ns after INPUT SELECT has become false.

The DATA IN signals must not be assumed to be correct until at least 500 ns after REPLY becomes true; INPUT SELECT must not be set false until the DATA IN signals have been staticized within the computer.

INPUT SELECT must not be set true until at least 200 ns after REPLY has returned to FALSE.

(2) Peripheral

REPLY must not be set true until the DATA IN signals have been set correctly. DATA IN must be set ZERO by the time REPLY is set false.

4.2 Single word output (see Figure 2)

Computer

The ADDRESS and DATA OUT signals must be in the correct state at least 200 ns before OUTPUT SELECT is set true and must remain correct until at least 200 ns after OUTPUT SELECT is set false again. The latter event must not occur until at least 500 ns after REPLY has become true.

OUTPUT SELECT must not be set true until at least 200 ns after REPLY has become false.

4.3 Block input (see Figure 3)

(1) Computer

The ADDRESS signals must be in the correct state at least 200 ns before BLOCK TRANSFER is set true and must remain correct until at least 200 ns after BLOCK TRANSFER is set false.

BLOCK TRANSFER must be true at least 200 ns before INPUT SELECT is set true for the first word and must remain true until at least 200 ns after INPUT SELECT is set false after the last word transfer.

The DATA IN signals must not be assumed to be correct until at least 500 ns after REPLY becomes true.

INPUT SELECT must not be again set true until at least 200 ns after REPLY has returned false.

The LAST WORD signal must be correct at least 200 ns before INPUT SELECT goes true and must remain correct until at least 200 ns after INPUT SELECT becomes false again.

(2) Peripheral

REPLY must not be set true until the DATA IN signals have been set correctly.

DATA IN lines must be set to zero not more than 200 ns after BLOCK TRANSFER has been set false.

4.4 Block output (see Figure 4)

Computer

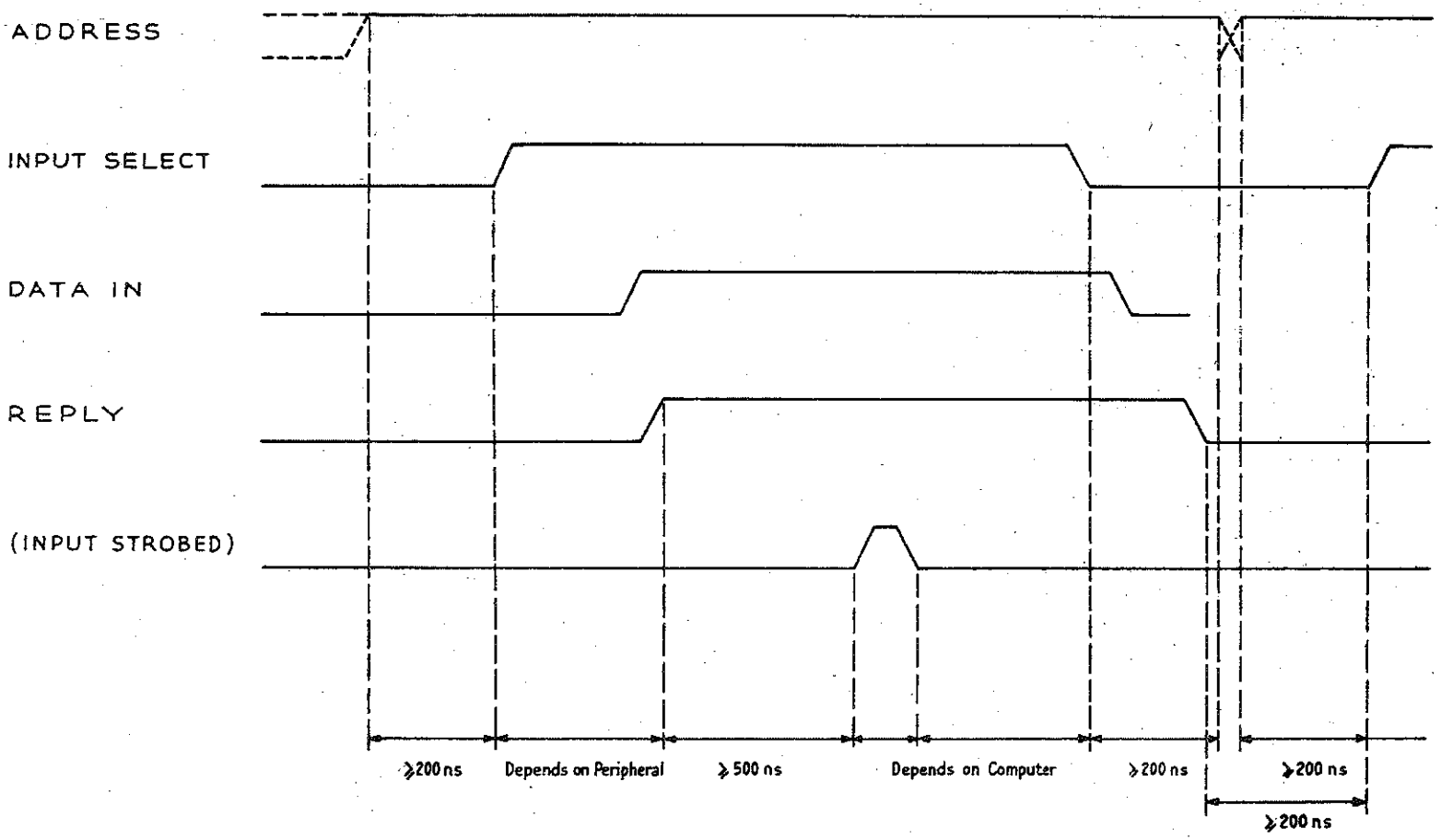
The ADDRESS signals must be in the correct state at least 200 ns before BLOCK TRANSFER is set true and must remain correct until at least 200 ns after BLOCK TRANSFER is set false.

OUTPUT SELECT must not be set true for the first word until at least 200 ns after BLOCK TRANSFER has been set true; BLOCK TRANSFER must not be set false until at least 200 ns after OUTPUT SELECT has been set false for the last time.

The DATA OUT lines must be correct at least 200 ns before OUTPUT SELECT is set true and must remain correct until at least 200 ns after OUTPUT SELECT has been set false again.

OUTPUT SELECT must not be set false until at least 500 ns after REPLY has become true, and must not be set true again until at least 200 ns after REPLY has returned to false.

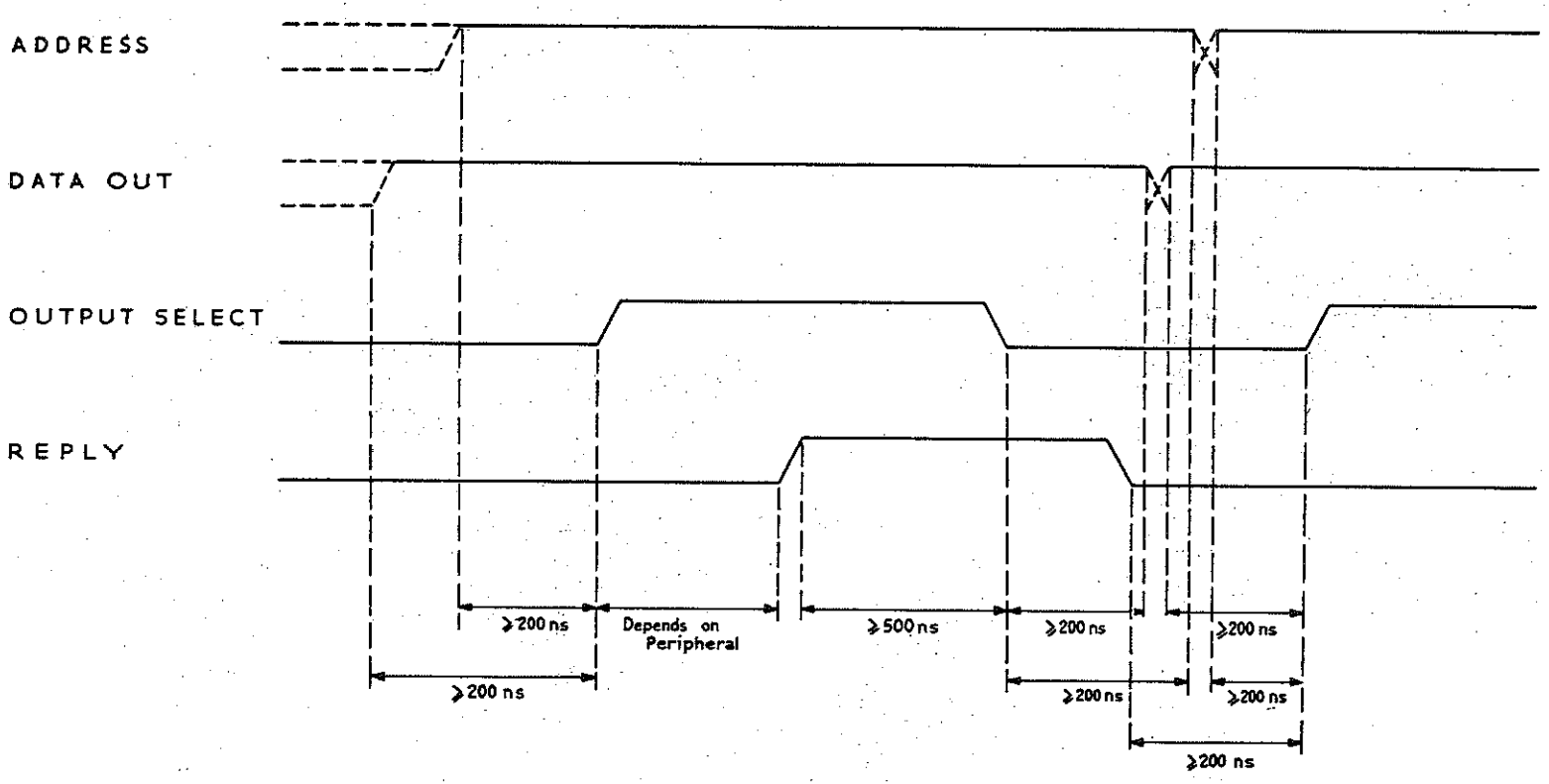
The LAST WORD signal must be correct at least 200 ns before OUTPUT SELECT is set true.



900 series INTERFACE
SINGLE WORD INPUT TIMING

Figure 1 (issue 2)

Figure 2 *(Issue 2)*



900 series INTERFACE
SINGLE WORD OUTPUT TIMING

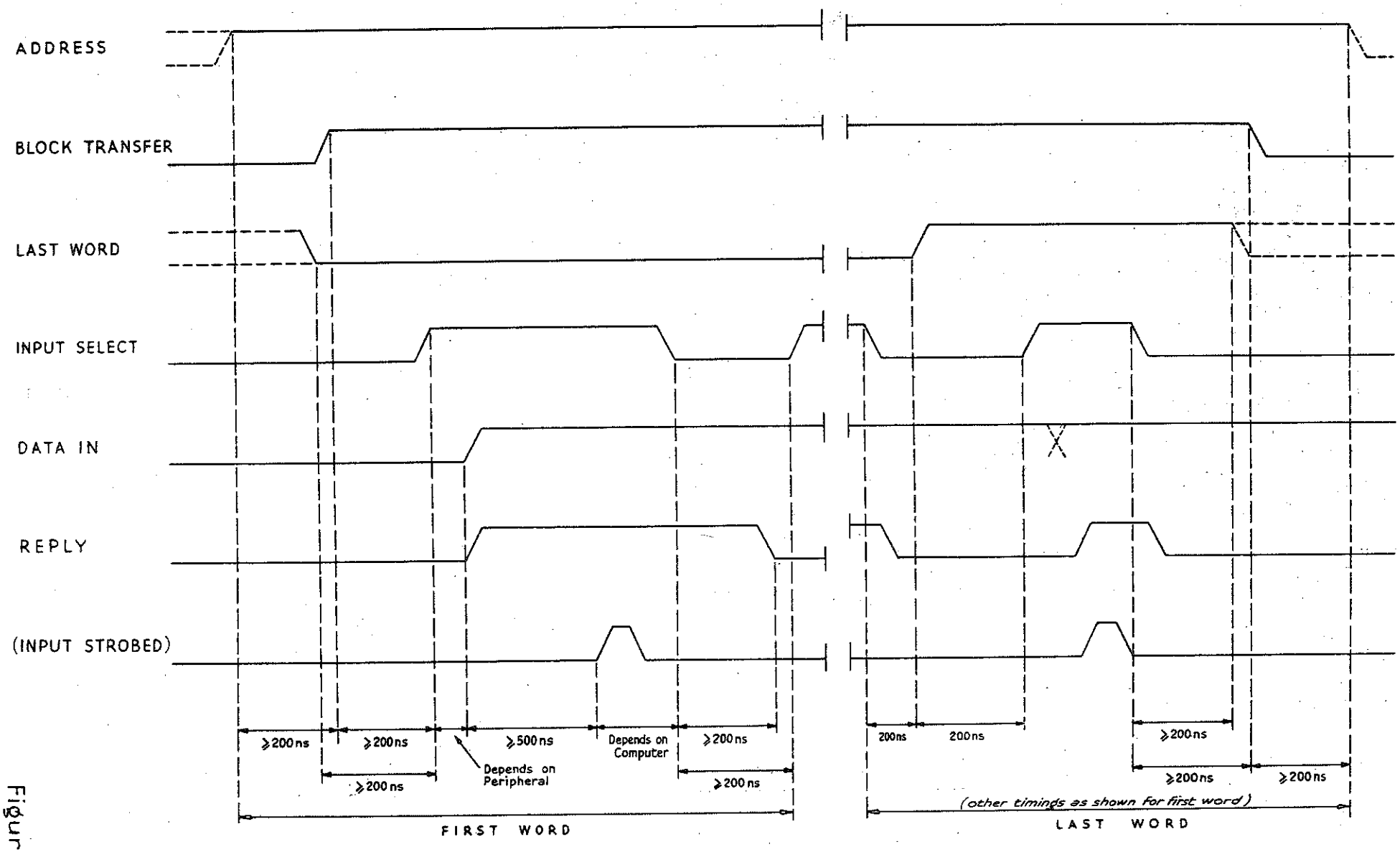
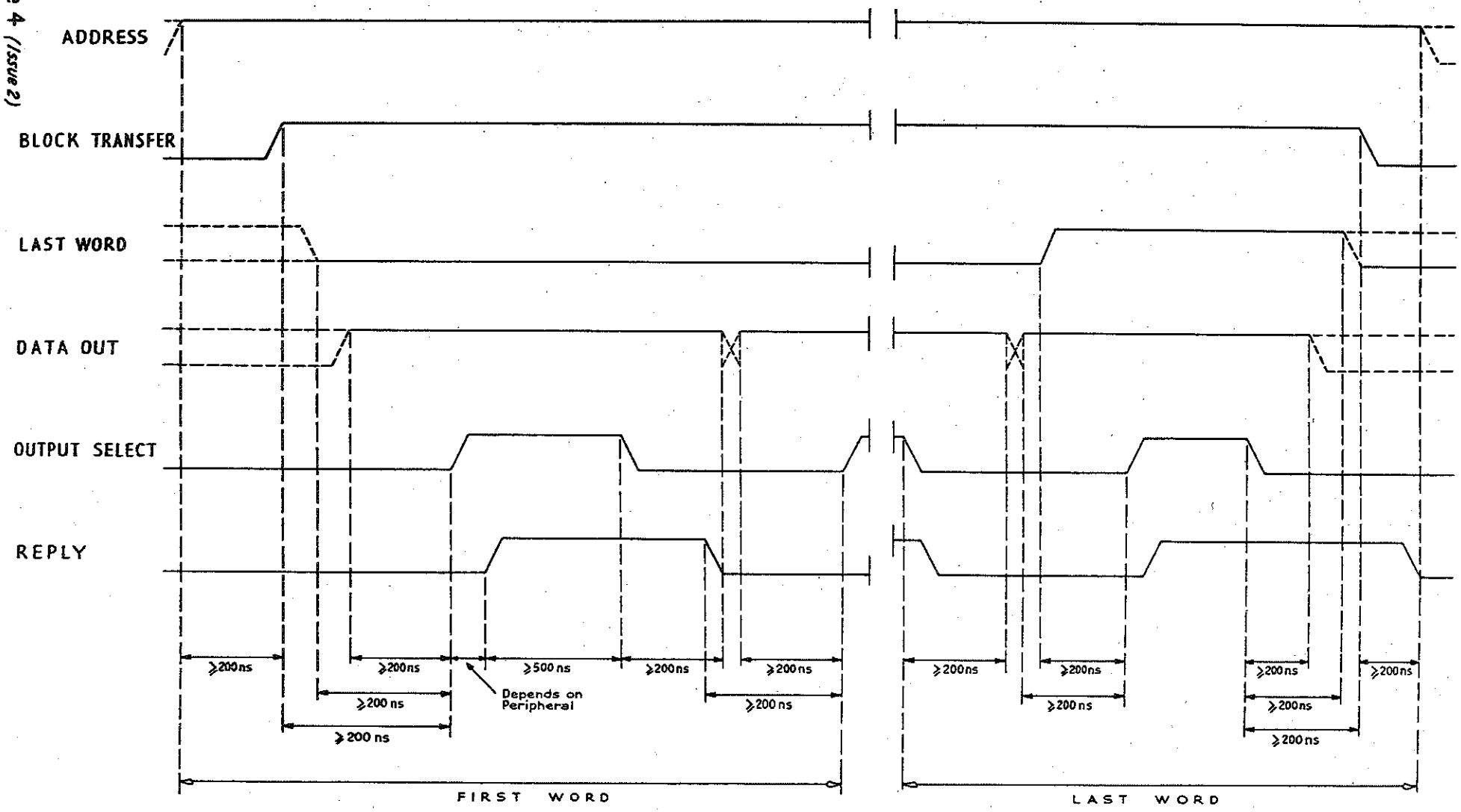


Figure 3 *(Issue 2)*

900 series INTERFACE
BLOCK INPUT TIMING

900
1.2.7.

Figure 4 *(Issue 2)*



900 series INTERFACE
BLOCK OUTPUT TIMING